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| 09/691,756 | 10/18/2000 | Robert Castellano | 61607-1550 | 3872 |

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| EXAMINER | |
|---|---|
| MOLINARI, MICHAEL J | |
| **ART UNIT** | **PAPER NUMBER** |
| 2665 | |

DATE MAILED: 04/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/691,756 | CASTELLANO, ROBERT | |
| | Examiner | Art Unit | |
| | Michael J Molinari | 2665 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *17 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Objections*

1. Claims 15 and 44 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The fact that an address "can be of any length" does not further limit the parent claim.

2. Claim 38 is objected to because of the following informalities: The first line states "wherein said of said plurality of conditions...", which is unclear. Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Regarding claims 15 and 44, the phrase "can be" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

### *Claim Rejections - 35 USC § 102*

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-44 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamanaka (U.S. Patent No. 6,693,911).

7. Referring to claim 1, Yamanaka discloses a system for transmitting and receiving information, said system comprising: a first layer transceiver device (ATM Layer Device, see column 2, lines 41-47); a plurality of second layer transceiver devices (PHY Layer Devices, see column 2, lines 41-47); and an interface connecting said first layer transceiver device and said plurality of second layer transceiver devices (Level 2 UTOPIA Interface, see column 2, lines 41-47), wherein said first layer transceiver device and said plurality of second layer transceiver devices transmit and receive said information across said interface (see column 3, lines 5-11), wherein said information comprises data and a time division multiplexed (TDM) signal (see Figure 7), wherein said TDM signal indicates the availability of one of said second layer transceiver devices (see column 3, lines 5-11).

8. Referring to claim 2, Yamanaka discloses that the TDM signal comprises a transmit available indicator of whether one of said plurality of second layer transceiver devices can receive said information from said first layer transceiver (see column 3, lines 5-11).

9. Referring to claim 3, Yamanaka discloses that said TDM signal comprises a receive available indicator of whether one of said plurality of second layer transceiver devices can transmit said information to said first layer transceiver (see column 3, lines 5-11).

10. Referring to claim 4, Yamanaka discloses that a first second layer transceiver device of said plurality of second layer transceiver devices is granted access to write said availability to said TDM signal, said access based on a plurality of conditions (see column 3, lines 5-11 and lines 45-47 and column 4, lines 9-11 and lines 53-67).

11. Referring to claim 5, Yamanaka discloses that said plurality of conditions comprises a synchronization signal being detected as asserted on the edge of a reference clock and a certain amount of delay being expired (see column 3, lines 40-45 and 53-56, column 4, lines 19-22, and Figures 7 and 8).

12. Referring to claim 6, Yamanaka discloses that said certain amount of delay is a calculated amount of clock edges after assertion of said synchronization signal, said calculated amount equal to an address of said first second layer transceiver device minus one (see column 4, lines 32-34).

13. Referring to claim 7, Yamanaka discloses that said plurality of conditions comprises a speed access variable, said speed access variable allowing a high speed transceiver of said second layer transceiver device to write said availability multiple times during a synchronization period (see column 3, lines 33-37).

14. Referring to claim 8, Yamanaka discloses that said TDM signal is transmitted and received in-band along with said data over a stream (see column 3, lines 12-67 and column 4, lines 1-31).

15. Referring to claim 9, Yamanaka discloses that said TDM signal is transmitted out-of-band from said data in a plurality of separate signals (see Figure 5).

16. Referring to claim 10, Yamanaka discloses a system for transmitting and receiving information, said system comprising: a first layer transceiver device (ATM Layer Device, see column 2, lines 41-47); a plurality of second layer transceiver devices (PHY Layer Devices, see column 2, lines 41-47); an interface connecting said first layer transceiver device and said plurality of second layer transceiver devices (Level 2 UTOPIA Interface, see column 2, lines 48-50), wherein said first layer transceiver and said plurality of second layer transceiver devices transmit and receive said information across said interface (see column 3, lines 5-11); wherein said information comprises a plurality of data and a plurality of control signals to control the transmission and reception of said information over said interface (see Figure 5 and see column 3, lines 5-67 and column 4, lines 1-27); and a protocol data unit (PDU) for data transfer of said information (Cell, see column 2, lines 58-61), wherein said PDU comprises an address for one of said plurality of second layer transceiver devices (see column 10, lines 34-48).

17. Referring to claim 11, Yamanaka discloses that said address is the destination address of one of said plurality of second layer transceiver devices for which said information in said PDU is intended (see column 10, lines 34-48).

18. Referring to claim 12, Yamanaka discloses that said address is the source address of one of said plurality of second layer transceiver devices from which said information in said PDU originated (see column 10, lines 34-48).

19. Referring to claim 13, Yamanaka discloses that said PDU comprises a header portion (see Figures 4A and 4B and see column 2, lines 62-66), a user defined (UDF) portion (see column 2, lines 58-61), and a payload portion (see column 2, lines 62-66).

20. Referring to claim 14, Yamanaka discloses that said UDF portion comprises said address (see column 10, lines 34-48).

21. Referring to claim 15, Yamanaka discloses that said address can be of any length (see column 10, lines 34-48).

22. Referring to claim 16, Yamanaka discloses a system for transmitting and receiving information, said system comprising: an ATM layer transceiver device (ATM Layer Device, see column 2, lines 41-47); a plurality of physical layer transceiver devices (PHY Layer Devices, see column 2, lines 41-47); and an ATM to physical layer interface module connecting said ATM layer transceiver device and said plurality of physical layer transceiver devices (Level 2 UTOPIA Interface, see column 2, lines 48-50), wherein said ATM layer transceiver device and said plurality of physical layer transceiver devices transmit and receive said information across said ATM to physical layer interface module (see column 3, lines 5-11), wherein said information comprises a plurality of data and a plurality of control signals to control the transmission and reception of said information over said ATM to physical layer interface module (see Figure 5 and see column 3, lines 5-67 and column 4, lines 1-27), wherein at least one of said plurality of control signals is a time division multiplexed (TDM) signal (see Figure 7).

23. Referring to claim 17, Yamanaka discloses that said time division multiplexed signal indicates the cell availability of one of said physical layer transceiver devices (see column 3, lines 5-11).

24. Referring to claim 18, Yamanaka discloses that said time division multiplexed signal comprises a transmit cell available (TxClav) indicator of whether one of said plurality of physical layer transceiver devices can receive said information (see column 3, lines 5-11).

25. Referring to claim 19, Yamanaka discloses that said time division multiplexed signal comprises a receive cell available (RxClav) indicator of whether one of said plurality of physical layer transceiver devices can transmit said information (see column 3, lines 5-11).

26. Referring to claim 20, Yamanaka discloses that a first physical layer transceiver device of said plurality of physical layer transceiver devices is granted access to write said availability to said time division multiplexed signal, said access based upon a plurality of conditions (see column 3, lines 5-11 and lines 45-47 and column 4, lines 9-11 and lines 53-67).

27. Referring to claim 21, Yamanaka discloses that said plurality of conditions comprises a synchronization signal being detected as asserted on the edge of a reference clock and a certain amount of delay being expired (see column 3, lines 40-45 and 53-56, column 4, lines 19-22, and Figures 7 and 8).

28. Referring to claim 22, Yamanaka discloses that said certain amount of delay is a calculated amount of clock edges after assertion of said synchronization signal (see column 4, lines 32-34).

29. Referring to claim 23, Yamanaka discloses that said calculated amount is equal to an address of said first physical layer transceiver device minus one (see column 4, lines 32-34).

30. Referring to claim 24, Yamanaka discloses that said ATM to physical interface module comprises an ATM layer cell availability status device and a physical layer cell availability status device (see Figure 5).

31. Referring to claim 25, Yamanaka discloses that said ATM layer cell availability status device communicates with said ATM layer and said physical layer cell availability status device (see Figure 5).

32. Referring to claim 26, Yamanaka discloses that said communication between said physical layer cell availability status device and said ATM layer cell availability status device comprises a plurality of interface control signals and interface data (see Figure 5).

33. Referring to claim 27, Yamanaka discloses that a first of said plurality of interface control signals is said TDM signal (see column 3, lines 12-67 and column 4, lines 1-31).

34. Referring to claim 28, Yamanaka discloses that a second of said plurality of control signals is said synchronization signal and a third of said plurality of control signals is said reference clock (see column 3, lines 12-67 and column 4, lines 1-31).

35. Referring to claim 29, Yamanaka discloses that said interface data is a protocol data unit (PDU) (Cell, see column 2, lines 58-61).

36. Referring to claim 30, Yamanaka discloses that said PDU comprises a header portion (see Figures 4A and 4B and see column 2, lines 62-66), a user defined (UDF) portion (see column 2, lines 58-61), and a payload portion (see column 2, lines 62-66).

37. Referring to claim 31, Yamanaka discloses that said UDF portion comprises said address (see column 10, lines 34-48).

38. Referring to claim 32, Yamanaka discloses a method for transmitting and receiving information, said method comprising the steps of: implementing a first layer transceiver device (ATM Layer Device, see column 2, lines 41-47); implementing a plurality if second layer transceiver devices (PHY Layer Devices, see column 2, lines 41-47); and providing an interface connecting said first layer transceiver device and said plurality of second layer transceiver devices (Level 2 UTOPIA Interface, see column 2, lines 48-50), wherein said first layer transceiver device and said plurality of second layer transceiver devices transmit and receive said

information across said interface (see column 3, lines 5-11), wherein said information comprises data and a time division multiplexed (TDM) signal (see Figure 7), wherein said TDM signal indicates the availability of one of said second layer transceiver devices (see column 3, lines 5-11).

39. Referring to claim 33, Yamanaka discloses that said TDM signal comprises a transmit available indicator of whether one of said plurality of second layer transceiver devices can receive said information (see column 3, lines 5-11).

40. Referring to claim 34, Yamanaka discloses that said TDM signal comprises a receive available indicator of whether one of said plurality of second layer transceiver devices can transmit said information (see column 3, lines 5-11).

41. Referring to claim 35, Yamanaka discloses that a first second layer transceiver device of said plurality of second layer transceiver devices is granted access to write said availability to said TDM signal, said access based on a plurality of conditions (see column 3, lines 5-11 and lines 45-47 and column 4, lines 9-11 and lines 53-67).

42. Referring to claim 36, Yamanaka discloses that said plurality of conditions comprises a synchronization signal being detected as asserted on the edge of a reference clock and a certain amount of delay being expired (see column 3, lines 40-45 and 53-56, column 4, lines 19-22, and Figures 7 and 8).

43. Referring to claim 37, Yamanaka discloses that said certain amount of delay is a calculated amount of clock edges after assertion of said synchronization signal, said calculated amount equal to an address of said first second layer transceiver device minus one (see column 4, lines 32-34).

44. Referring to claim 38, Yamanaka discloses that said plurality of conditions comprises a speed access variable, said speed access variable allowing a high speed transceiver of said second layer transceiver device to write said availability multiple times during a synchronization period (see column 3, lines 33-37).

45. Referring to claim 39, Yamanaka discloses a method for transmitting and receiving information, said method comprising the steps of: implementing a first layer transceiver device (ATM Layer Device, see column 2, lines 41-47); implementing a plurality of second layer transceiver devices (PHY Layer Devices, see column 2, lines 41-47); providing an interface connecting said first layer transceiver device and said plurality of second layer transceiver devices (Level 2 UTOPIA Interface, see column 2, lines 48-50), wherein said first layer transceiver device and said plurality of second layer transceiver devices transmit and receive said information across said interface (see column 3, lines 5-11); providing a plurality of control signals to control the transmission and reception of said information over said interface (see Figure 5 and see column 3, lines 5-67 and column 4, lines 1-27); and implementing a protocol data unit (PDU) for data transfer of said information (Cell, see column 2, lines 58-61), wherein said PDU comprises an address for one of said plurality of second layer transceiver devices (see column 10, lines 34-48).

46. Referring to claim 40, Yamanaka discloses that said address is the destination address of one of said plurality of second layer transceiver devices for which said information in said PDU is intended (see column 10, lines 34-48).

47. Referring to claim 41, Yamanaka discloses that said address is the source address of one of said plurality of second layer transceiver devices from which said information in said PDU originated (see column 10, lines 34-48).

48. Referring to claim 42, Yamanaka discloses that said PDU comprises a header portion (see Figures 4A and 4B and see column 2, lines 62-66), a user defined (UDF) portion (see column 2, lines 58-61), and a payload portion (see column 2, lines 62-66).

49. Referring to claim 43, Yamanaka discloses that said UDF portion comprises said address (see column 10, lines 34-48).

50. Referring to claim 44, Yamanaka discloses that said address can be of any length (see column 10, lines 34-48).

***Conclusion***

51. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

52. U.S. Patent No. 5,754,941 to Sharpe et al. teaches a method of using a UTOPIA interface that describes cell routing across the interface.

53. U.S. Patent No. 5,418,786 to Loyer et al. teaches a method of communicating status bytes in a manner compatible with the UTOPIA protocol.

54. U.S. Patent No. 5,485,456 to Shtayer et al. teaches a method of coupling an ATM layer device to a plurality of physical layer devices in an ATM system.

55. U.S. Patent No. 5,568,470 to Ben-Nun et al. teaches a method of transmitting ATM data across a physical interface to control latency.

56. U.S. Patent No. 5,784,370 to Rich teaches a method of regenerating a control signal at the UTOPIA interface between an ATM layer device and a PHY layer device.

57. U.S. Patent No. 5,875,192 to Cam et al. teaches an ATM inverse multiplexing system wherein data is communicated between ATM layer devices and physical layer devices.

58. U.S. Patent No. 5,894,476 to Fraser teaches an ATM layer device interface with reduced pin count.

59. U.S. Patent No. 6,307,858 to Mizukoshi et al. teaches a method of transmitting cells in an ATM system.

60. U.S. Patent No. 6,345,052 to Tse et al. teaches a method of transmitting status signals in an ATM system.

61. U.S. Patent No. 6,452,927 to Rich teaches a method of providing a serial interface between an ATM layer device and a physical layer device.

62. U.S. Patent No. 6,574,228 to Ganor et al. teaches a communication system with a method of communicating between a physical interface and a communication controller.

63. U.S. Patent No. 6,680,954 to Cam et al. teaches an ATM inverse multiplexing system comprising an ATM layer device and a physical layer device.

64. European Patent Application EP 0 949 839 A1 to NEC Corporation teaches an ATM cell transmission system that provides communication between an ATM level device and a plurality of physical layer devices.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J Molinari whose telephone number is (703) 305-5742. The examiner can normally be reached on Monday-Thursday 8am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (703) 308-6602. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MJM

Michael Joseph Molinari

ALPUS H. HSU
PRIMARY EXAMINER